COURSE
POWER ELECTRONICS
Modelling and Evaluation

2nd Semester 2017

Theory:

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Laboratory:

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Exercises:

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Theoretical Part – Planning and Evaluation

Lecture Time:
Monday: 9:40-11:20
Wednesday: 9:40-11:20

Course Objectives:

This course is primary designed for undergraduate student, with a strong background on electrical engineering and mathematics. The theoretical part of this course provides to the student a general background about important aspects of power electronics. This is an introduction course which presents the student an overview of all important aspects regarding power electronics topologies, different type of converters and modulation techniques. After the student has approved this course, the following specific goals are expected to be acquired:

- The student must be able to understand and recognize the operation of different semiconductors used in the industry nowadays.
- The student must be able to recognize and understand the operation of converter topologies such as rectifiers, inverters and DC/DC converters.
- The student must be able to understand modulation techniques applied to inverters such as PWM and SVM techniques.

Prerequisites:
Prerequisites of this course are defined by the Electrical Department of the Universidad e Santiago de Chile. Nevertheless, it is important the student has an undergraduate-level understanding of the following topics: Laplace and Fourier Transform, Bode Analysis and C programming.

Office Hours:
By appointment and after asking exercise assistants.

Main References:
Most of the content of our lecture can be found in the following book.

- Bin Wu, *High Power Converters and AC Drives*, Wiley IEEE Press, 2006.
  This book can be downloaded from: http://biblioteca.usach.cl/biblioteca-digital at ***myilibrary*** data base.

The following references can be used as complementary:

- Ned Mohan, *First Course on Power Electronics and Drives*, MNPERE, 2003.
- Muhammad Rashid, *Power Electronics Devices, Circuits, and Applications*, Pearson, 2014. This book can be downloaded from: http://biblioteca.usach.cl/biblioteca-digital at ***myilibrary*** data base.

Course Outline:

Table 1: Semester Lectures and Examination dates

Lecture	Date	Topic
01	07.08.2017	Course Presentation and Overview of Power Electronics
02	09.08.2017	Power Electronics Devices I (Diode, SCR, GCT, IGCT, MOSFET, IGBT)
03	14.08.2017	Power Electronics Devices II (Diode, SCR, GCT, IGCT, MOSFET, IGBT)
04	16.08.2017	Thermic circuits and heat sink design for Power Electronics Devices
05	21.08.2017	Multipulse Diode Rectifiers I
06	23.08.207	Multipulse Diode Rectifiers II
07	28.08.2017	Multipulse SCR Rectifiers I
08	30.08.2017	Multipulse SCR Rectifiers II
09	04.09.2017	Introduction to DC/DC Converters
10	06.09.2017	Ideal operation of Buck, Boost and Cuk converters
PEP1	09.09.2017	Saturday. From 9:30am to 12:50pm. Lectures 01 to 8
11	11.09.2017	Oral Examination1
12	13.09.2017	Steady-State equivalent circuit Modelling, losses and efficiency of DC/DC Converters.
13	18.09.2017	Holyday
13	20.09.2017	Discontinuous Conduction Mode in DC/DC Converters
14	25.09.2017	Converter Circuits and Transformer Isolation
15	27.09.2017	Converter Evaluation and Design
16	02.10.2017	Introduction to DC/AC Inverters and Space of Vectors
17	04.10.2017	Block Operation of 2-level Inverter I
18	09.10.2017	Holyday
19	11.10.2017	Block Operation of 2-Level Inverter II
20	16.10.2017	PWM for 2-level Inverters I
21	18.10.2017	PWM for 2-Level Inverters II
PEP2	21.10.2017	Saturday. From 9:30am to 12:50pm. Lectures 9-19
22	23.10.2017	Oral Examination 2
23	25.10.2017	Space Vector Modulation for Inverters I
24	30.10.2017	Space Vector Modulation for Inverters II
25	01.11.2017	Holyday
26	06.11.2017	Space Vector Modulation for Inverters III
27	08.11.2017	Introduction to 3-Level Neutral Point Clamped (NPC) Inverter
28	13.11.2017	Space Vector Modulation for NPC Inverter I
29	15.11.2017	Space Vector Modulation for NPC Inverter II
30	20.11.2017	Space Vector Modulation for NPC III
31	22.11.2017	Questions for PEP 3
PEP3	25.11.2017	Saturday. From 9:30am to 12:50pm. Lectures 20 to 30
32	27.11.2017	Oral Examination 3
33	29.11.2017	Recuperative PEPs for those who have miss one or more PEPs during the semester.
PA	02.12.2017	Saturday. From 9:30am to 12:50pm. Lectures 01 to 30

Grading Policy:

The theoretical part of this course is divided in three written examinations, evaluation of three homework and three Oral examinations. The weighing for each of these examinations are as follows:

- MARK1= HW1(10%), OE1(10%), EX1(10%), PEP1(80%).
- MARK2= HW2(10%), OE2(10%), EX2(10%), PEP2(80%).
- MARK3= HW3(10%), OE3(10%), EX3(10%), PEP3(80%).

Final Mark = (MARK1 + MARK2 + MARK3)/3

If (Final Mark≥4.0 && all MARKs≥4.0) ⇒ Approved
else if (Any MARK < 4.0 && Final Mark≥5.0) ⇒ Approved
else PA

In case of PA. The PA replace the worst MARK and have double weight, after that:

Final Mark = (MARK1 + MARK2 + MARK3 - min(MARK1,MARK2,MARK3)+2PA)/4

If Final Mark≥4.0 ⇒ Approved
Else See you next semester again.

PEP: Standard written examination. This evaluation is taken on Saturday and last 180min. (See Course Outline)
Homework (HW): One Homework is giving for students before each PEP. This Homework is very important to prepare each PEP. Students can make groups formed by up to 6 persons to solve the homework. Due date for each homework is presented in important dates. Homework has to be written by hand. No computer printed homework will be accepted.
Oral Examination(OE): One oral examination is taken for each student right after each PEP (see important dates). Oral examination is individual and last maximum 15min. The student can enter to the examination room with his solved homework and one question of the homework is taken randomly, which is later evaluated.
Exercise mark(EX): Individual evaluation performed during the simulation lectures, each EX takes in account the attendance, efficient use of time and achieve the goals defined for each lecture.

Important Dates:

PEP1	09.09.2017
Oral Examination 1	11.09.2017
Homework1	11.09.2017
PEP2	21.10.2017
Oral Examination 2	23.10.2017
Homework2	23.10.2017
PEP3	25.11.2017
Oral Examination 3	27.11.2017
Homework3	27.11.2017
PA	02.12.2017

Class Policy:

- Regular attendance is essential and expected.

Academic Honesty:
Lack of knowledge of the academic honesty policy is not a reasonable explanation for a violation. To copy in any way during examination is causal of expulsion of the University.

Exercise Part – Planning and Evaluation

Lecture Time:
Wednesday: 17:10 - 18:40
Thursday: 13:50-15:20

Course Objectives:

At the end of the exercise part of this course, the students must be able to:

- Perform general systems simulations and signal analysis using PLECS simulation software.
- Perform power electronics converters simulations using PLECS simulation software.
- Verify theoretical exercises results by means simulation with PLECS.
- Verify power electronics converters power stages design by means simulation with PLECS.

Course Outline:

Table 2: Semester Exercise Sessions dates

Lecture	Date	Topic
01	09.08.2017	Simulation (S0): Introduction to PLECS, basic configuration and devices use.
02	10.08.2017	Simulation (S0): Introduction to PLECS, basic configuration and devices use.
03	16.08.2017	Exercise: Losses in power electronics devices.
04	17.08.2017	Exercise: Losses in power electronics devices.
05	23.08.2017	Simulation (S1): Power losses on semiconductor devices and thermal simulation.
06	24.08.2017	Simulation (S1): Power losses on semiconductor devices and thermal simulation.
07	30.08.2017	Exercise : Diodes and thyristor rectifiers.
08	31.08.2017	Exercise: Diodes and thyristor rectifiers.
09	06.09.2017	Simulation (S2): Six Pulse Diodes and thyristor rectifiers.
10	07.09.2017	Simulation (S2): Six Pulse Diodes and thyristor rectifiers.
11	13.09.2017	Exercise: Analysis of DC-DC converters.
12	14.09.2017	Exercise: Analysis of DC-DC converters.
13	27.09.2017	Simulation (S3): Buck and Boost converters simulation.
14	28.09.2017	Simulation (S3): Buck and Boost converters simulation.
15	04.10.2017	Exercise: DCM operation of DC-DC converters and losses consideration.
16	05.10.2017	Exercise: DCM operation of DC-DC converters and losses consideration.
17	11.10.2017	Exercise: Block operation of two-level VSI.
18	12.10.2017	Exercise: Block operation of two-level VSI.
19	18.10.2017	Simulation (S4): Block operation and PWM applied to a two-level VSI.
20	19.10.2017	Simulation (S4): Block operation and PWM applied to a two-level VSI.
21	25.10.2017	Exercise: SVM for two-level VSI.
22	26.10.2017	Exercise: SVM for two-level VSI.
23	08.11.2017	Simulation (S5): SVM applied to a two-level VSI.
24	09.11.2017	Simulation (S5): SVM applied to a two-level VSI.
25	15.11.2017	Exercise: SVM for the NPC converter.
26	16.11.2017	Exercise: SVM for the NPC converter.
27	22.11.2017	Simulation (S6): SVM applied to a NPC converter.
28	23.11.2017	Simulation (S6): SVM applied to a NPC converter.

Grading Policy:

The exercise part of this course is divided in three evaluations, which are used for calculating each MARK of the theoretical part. The weighing for each of these examinations are as follows:

- EX1= S1(50%), S2(50%).
- EX2= S3(50%), S4(50%).
- EX3= S5(50%), S6(50%).

Simulation work (S): The evaluation performed during the simulation session, the mark is calculated as follows: The attendance to the session gives the student a 4.0, when the student achieves an progress point (defined on each session guide) the mark goes up to 5.5; if the student finishes the activities within the the session time, he gets a 7.0. If the student does not attend to the session, he gets an 1.0.

Experimental Part – Planning and Evaluation

Lab Time:
Group A1 Wednesday: 17:10-20:10
Group A2 Friday: 8:00-11:10
Group B1 Friday: 11:20-15:20
Group B2 Friday: 18:45-21:35

Course Objectives:
This is an experimental course which presents the student, through different laboratory experiences, the operation and behaviour of different power electronics devices. Also, this course provides to the student a general background about software to program a Digital Signal Processor and CPLD, using Code Composer (C) and Quartus (VHDL) respectively. After the student has approved this course, the following specific goals are expected to be acquired:

- The student must be able to understand measurement and protection circuit in power electronics devices.
- The student must be able to program a DSP and CPLD applied to the operation of converter topologies such as rectifiers, inverters and DC/DC converters.

Prerequisites:
Prerequisites of this course are defined by the Electrical Department of the Universidad de Santiago de Chile. Nevertheless, it is important the student has an undergraduate-level understanding of the following topics: VHDL and C programming.

Office Hours:
By appointment.

Course Outline:

Table 3: Lab Experiences dates

Lab	Group	Date	Topic
01	A1-1	30.08.2017	Measurement, Protection and Digital Signal Processor
01	A2-1	01.09.2017	Measurement, Protection and Digital Signal Processor
01	B1-1	01.09.2017	Measurement, Protection and Digital Signal Processor
01	B2-1	01.09.2017	Measurement, Protection and Digital Signal Processor
01	A1-2	06.09.2017	Measurement, Protection and Digital Signal Processor
01	A2-2	08.09.2017	Measurement, Protection and Digital Signal Processor
01	B1-2	08.09.2017	Measurement, Protection and Digital Signal Processor
01	B2-2	08.09.2017	Measurement, Protection and Digital Signal Processor
02	A1-1	13.09.2017	Sampling Time and CPLD
02	A2-1	15.09.2017	Sampling Time and CPLD
02	B1-1	15.09.2017	Sampling Time and CPLD
02	B2-1	15.09.2017	Sampling Time and CPLD
02	A1-2	27.09.2017	Sampling Time and CPLD
02	A2-2	29.09.2017	Sampling Time and CPLD
02	B1-2	29.09.2017	Sampling Time and CPLD
02	B2-2	29.09.2017	Sampling Time and CPLD
03	A1-1	04.10.2017	SPI Communication
03	A2-1	06.10.2017	SPI Communication
03	B1-1	06.10.2017	SPI Communication
03	B2-1	06.10.2017	SPI Communication
03	A1-2	11.10.2017	SPI Communication
03	A2-2	13.10.2017	SPI Communication
03	B1-2	13.10.2017	SPI Communication
03	B2-2	13.10.2017	SPI Communication
04	A1-1	18.10.2017	Rectifier
04	A2-1	20.10.2017	Rectifier
04	B1-1	20.10.2017	Rectifier
04	B2-1	20.10.2017	Rectifier
04	A1-2	25.10.2017	Rectifier
04	A2-2	03.11.2017	Rectifier
04	B1-2	03.11.2017	Rectifier
04	B2-2	03.11.2017	Rectifier
05	A1-1	08.11.2017	Booster
05	A2-1	10.11.2017	Booster
05	B1-1	10.11.2017	Booster
05	B2-1	10.11.2017	Booster
05	A1-2	15.11.2017	Booster
05	A2-2	17.11.2017	Booster
05	B1-2	17.11.2017	Booster
05	B2-2	17.11.2017	Booster
Rec	A1-1	22.11.2017	Recovery Lab
Rec	A2-1	24.11.2017	Recovery Lab
Rec	B1-1	24.11.2017	Recovery Lab
Rec	B1-1	24.11.2017	Recovery Lab
Rec	A1-2	29.11.2017	Recovery Lab
Rec	A2-2	01.12.2017	Recovery Lab
Rec	B1-2	01.12.2017	Recovery Lab
Rec	B2-2	01.12.2017	Recovery Lab

Grading Policy:

Each Lab experience is divided in three evaluations: Pre-Report, Entrance Test and Final Report. The weighing for each of these examinations are as follows:

LABx= PRx·0.35+ ETx·0.3+ FRx·0.35

Final Mark = LAB1· 0.2+LAB2· 0.2+LAB3· 0.2+LAB4· 0.2+LAB5· 0.2
(LAB Rec can replace one LABx).

If (Final Mark≥4.0 && all LABx≥4.0) ⇒ Approved
else See you next semester

Pre-Report (PR): One Pre-Report is giving for students before each Lab Experience. The day of Lab each group must deliver the pre-report resolved. Pre-Report has to be written by hand. No computer printed report is accepted. If PRx<4.0 group can't enter Lab and LABx =1.0
Entrance Test (ET): Standar written test. This evaluation is taken before the Lab experience. Examination is individual and last maximum 20min. If ETx<4.0 student can't enter Lab and LABx =1.0
Final Report(FR): One Final-Report is request one week after Lab Experience. Pre-Report has to be written by hand. No computer printed report is accepted.